REMARKS

Applicant's thank the Examiner for his time extended on <<proposed telephone conference>> in which various embodiments of the present invention were discussed relative to the prior art.

Claim 5-7 and 9 are pending.

Claim 5 has been amended.

Claims 5-7 and 9 remain.

Reconsideration is respectfully requested.

Applicant's time to respond:

The last Office Action was mailed July 15, 2002. The initial 3 month deadline for responding without having to pay a penalty ends on October 15, 2002.

In determining whether this document is timely filed, the USA Patent Office is asked to note the applicant's Certificate of Mailing in conjunction with 37 CFR §1.8.

The Patentability of Claims 5-7 and 9 Over the Prior Art:

Claims 5-7 and 9 were rejected under 35 USC §103(a) as being unpatentable over Subramanian et al. (5,668,021) in view of "Applicant Admitted Prior Art" (AAPA).

Applicants respectfully traverse.

Independent claim 5 sets forth a pull-up transistor comprising a semiconductor substrate of a first conductivity type with source and drains regions of second conductivity type formed in the substrate to define a channel therebetween. One of the source and drain regions is electrically coupled to an I/O pad and the other is electrically coupled to a Vdd terminal. A first sector of the channel region comprises an impurity region with impurities of second conductivity type, which also comprises a surface region of the second conductivity type as a depletion channel. A second sector of the channel region exclusive of the first sector comprises a uniform doping concentration of the first conductivity type and a surface region thereof of the first conductivity type as an enhancement channel. A gate insulating layer is over at least a portion of the surface regions of the first and second sectors and a gate is disposed on the gate insulating layer over at least a portion of the first and second sectors.

Subramanian teaches a method of fabricating a MOS device with a **buried** channel 24. (See abstract and FIG. 7 of Subramanian).

In forming such device, Subramanian teaches providing an opening 18 in an insulating layer 16 (column 3, lines 16-32 with reference to FIG. 1). After forming the opening, spacers 22 may be formed against sidewalls of insulating layer 16 that define the opening. Subramanian teaches forming the spacers with a thickness of about **300-1000** angstroms (column 3, lines 33-49 with reference to FIG. 2). After forming the spacers, ions of a dopant species are implanted to *penetrate into* the semiconductor substrate 10 (emphasis added, column3, lines 50-54) to form *buried* junction region 24. The opening or gap between the spacers defines the lateral extend of the buried channel. In subsequent steps, the opening between spacers 22 is filled with gate poly. It may be noted that the thickness of spacers 22 will establish the lateral distance between ends of the buried channel and respective source and drain regions of the MOSFET.

After forming a gate structure of poly 26 between spacers 22, insulating layer 16 is removed (column 4, lines 39-40 with reference to FIG. 4). Next, lightly doped source and drain regions 28,30 may be formed (column 5, lines 1-4 and referencing FIGS. 5-6). Second sidewall spacers 32 are then formed against sidewalls of the gate structure comprising the first sidewall spacers 22, after which heavily doped source and drain regions 34,36 may be formed. Accordingly, Subramanian teaches a thickness for the spacers 22 of about 300-1000 angstroms, which in-turn define a lateral distance between an edge of the lightly doped source and drain regions 30,28 and respective edges of buried junction 24.

With Subramanian teaching a buried channel, applicant submits that Subramanian teaches away from the depletion and enhancement channels of the respective first and second sectors as set forth in claim 5 of the present application. In fact, Subramanian discloses benefits of a buried channel that include reducing electric fields in a channel region of the MOS device of a buried channel (column 1, lines 28-32). In this context, it may be noted that the buried channel is *buried*. Thus, Subramanian teaches away from the surface region of second conductivity type as a depletion channel as set forth in claim 5.

Further, assuming arguendo that that the buried channel of Subramanian were not buried, but instead might reside at the surface as suggested by the Examiner; then applicant submits (pursuant such assumption for purposes of argument) that the device would be inoperative as a pull-up transistor between an I/O pad and a Vdd terminal as set forth in claim 5. Such device would comprise such low breakdown voltage and insufficient isolation so as to render it worthless between an I/O pad and Vdd terminal – e.g., as a pull-up transistor such as that set forth in claim 5.

Again, Subramanian teaches forming the buried channel by implanting ions through an opening between spacers 22. Subsequently, lightly doped source and drain regions may be defined in the substrate at sides of the spacers outside the previously defined opening. Accordingly, the thickness of spacers 22 define the relative lateral distance between the two regions. If the buried channel were not buried, but were instead to reside at the surface (in accordance with the Examiner's implication), then the narrow gap between the regions would not support voltage levels expected of a pull-up transistor as set forth in claim 5. Applicants submit that a separation distance of only 300-1000 angstroms (per spacers 22) between the two regions would render the device worthless as a pull-up transistor. With such narrow distance between the regions, the isolation and/or voltage tolerance of the resulting device would, applicants submit, be so low so as to render the device inoperative as a pull-up transistor. [1,2] [Copies of reference materials are enclosed herewith for convenience of the Examiner.]

Accordingly, applicant submits that the device of the Examiner's construction would be so vulnerable to voltage breakdown or punch through so as to be inoperable as a pull-up transistor.

Applicant further submits that this inoperable aspect of the assumed construction further highlights Subramanian's actual teachings of a "buried channel"; and that this further emphasizes Subramanian's teachings away from the embodiment of the present invention as set forth in claim 5.

Because Subramanian is related to the art of buried channel MOS transistors, does not disclose or suggest of a depletion channel for a pull-up transistor as set forth in claim 5, does not disclose or suggest difficulties, let alone need to improve pull-up transisitors, and because the Examiner's implied construct of Subramanian would not be operative as a pull-up transistor as set forth in claim 5, and, in deed, because Subramanian teaches away from features of embodiments of the present invention as set forth in claim 5; applicant submits that claim 5 is patentable over Subramanian.

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[1] See Gray, *Analysis and Design of Analog Integrated Circuits*, 2nd edition, p. 135 (John Wiley and Sons 1984) (Characterizing a typical substrate doping density of 10^15 atoms/cm^3 for an *n*-channel transistor).

[2] See Zeghbroeck, *Principles of Semiconductor Devices*, Fig. 4x and section 4.7.2 (© Bart Van Zeghbroeck 1997, via University of Colorado website updated August 2001 at http://ece-www.colorado.edu/~bart/book/breakdown.htm) (Showing a spherical structure having a breakdown less than about 2 volts for a density of 10^15; but a depletion width greater than about 3,000 angstroms or greater than about 3 x 10^-5 cm per the logarithmic scale. It may be said, therefore, that a depletion width greater than 1,000 angstroms would be required to support such breakdown voltages regardless of the structure).

Furthermore, applicant traverses in general other comments of the Examiner. For Example, applicant traverses the Examiner's characterization of certain portions of applicant's application and use thereof in building "prior art." At page 4, lines 16-17, the Examiner states that "[t]he combination is motivated by the teachings of AAPA . . ."

Again, applicant respectfully submits that motivation in forming combinations must come from the prior art absent teachings of applicant. Applicant submits that applicant's own perceptions (e.g., perception of difficulties in exemplary conventional devices) are not necessarily deemed a part of the prior art. Applicant's background section within the present application sets forth some observations of applicant regarding certain conventional devices and further teaches opinions of applicant regarding needs to improve pull-up transistors. Such opinions of applicant within the teachings of the present application is of the applicant; they are not specific expressions that the prior art may understand or have adopted applicant's perspectives. Thus, applicant respectfully traverses the Examiner's characterization of these teachings and perspectives of applicant as prior art.

Again, because the prior art does not disclose or suggest the features of the present invention as set forth in claim 5 it is submitted that claim 5 is patentable over the prior art. Likewise, it follows that dependent claims 6-7 and 9 also are patentable for reason of being dependent upon a patentable base claim and also for their own features.

In view of the above amendments and remarks, applicant submits that claims 5-7 and 9 of the present application are allowable and respectfully requests such action for this case.

The Examiner is encouraged to telephone the undersigned at (503)222-3613 if it appears that an interview would be helpful.

Respectfully submitted,
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ON 10-14-02

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

5. (Thrice Amended) A pull-up transistor disposed between a Vdd terminal and an I/O pad of a semiconductor device comprising:

a semiconductor substrate of a first [conductive-] conductivity type;

a source region and a drain region of a second [conductive] conductivity type formed in the substrate and defining between them a channel region, one of the source region and the drain region being electrically coupled to the I/O pad, the other one of the source region and the drain region being electrically coupled to the Vdd terminal;

an impurity implantation region of impurities of a second [conductive-] conductivity type formed in a first sector of the channel region, the first sector not reaching either one of the source region and the drain region;

the impurity implantation region of the first sector comprising a surface region [~~operable under field effect as~~] of the second conductivity type as a depletion channel;

a second sector of the channel region exclusive of the first sector comprising a uniform doping concentration of the first [conductive] conductivity type and a surface region [~~operable under field effect as~~] of the first conductivity type as an enhancement channel;

a gate insulating layer on the substrate over at least a portion of the surface region of the first sector and the surface region of the second sector; and

a gate on the gate insulating layer over at least a portion of the first sector and over at least a portion of the second sector.

7. (Amended) The transistor of claim 5, in which

the gate comprises a first portion over the first sector and a second portion over the second sector; and

the first portion is in a predetermined ratio with respect to the second portion.